MICROELECTRONIC CONTROLLING OF REALTIME COMPLICATED TECHNICAL SYSTEMS

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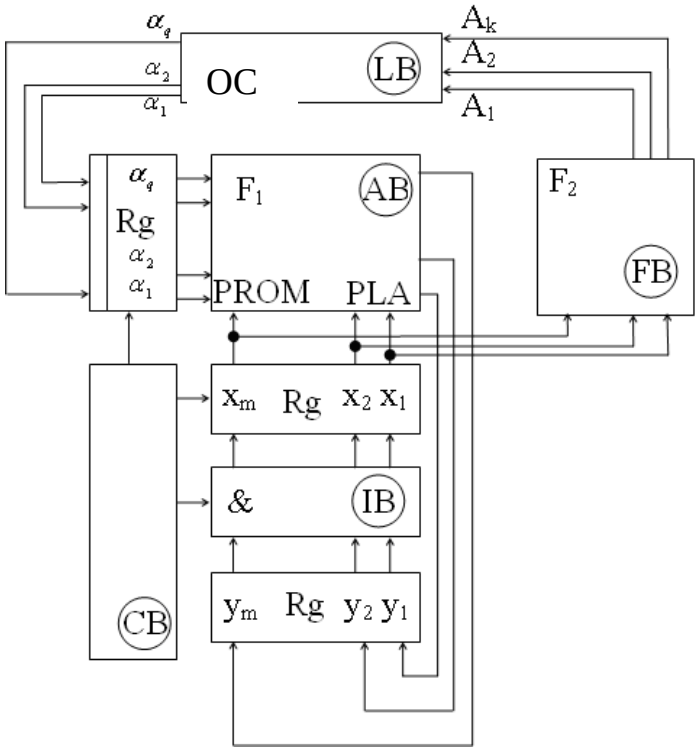
The very important parameter of high-speed realtime automation facilities is simplicity and reliability of control subsystems. For classical structure of Moore micro-programmed automatons (MPA), the operation algorithms are described as follows:

$$a(t+1) = F_1(a(t), \{\alpha\}) ; A(t) = F_2(a(t)) \quad (1)$$

where a(t) and a(t+1) are present (t) and following (t+1) state of the automaton; {α} – α_1, α_2,…α_q – logical preconditions; A(t) – A_1, A_2,…A_k –MPA output commands; F1 and F2 - Boolean function systems of MPA transitions and outputs.

Fig. 1 depicts a scheme of the automaton corresponding to equations (1); fig. 2 – control algorithm flow-graph (AFG) and fig. 3 – transition graph of Moore automaton. Algorithm of transition from AFG to the graph is presented in fig. 1. For simple MPA with number of states ≤32 and number of logical preconditions q≤5, capacity of programmable read only memory (PROM) does not exceed 5 kbit. Memory capacity (V) required for realization of Boolean function systems of transitions F1 shall be as $V(F)=m2^{m+q}$, where: m – length of representation code a(t) and a(t+1). When realizing more complicated automatons: with m=5, q=10, PROM=160kbit and m=6, q=16, PROM =24Mbit. Such memory capacity is too large for high-speed realtime automatons.



LB – logical block
OC – object of control
AB – address block
CB – control block
Rg – register of memory
FB – functional block
IB – informational block

Figure 1. Structural scheme of Moore automaton

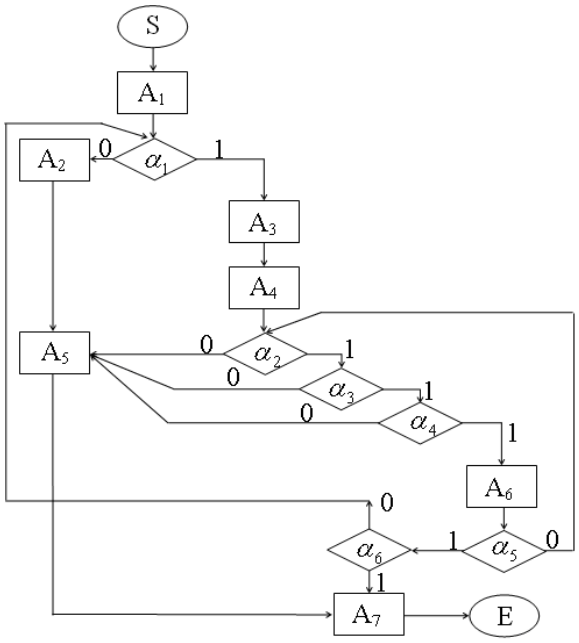


Figure 2. Flow-graph of control algorithm

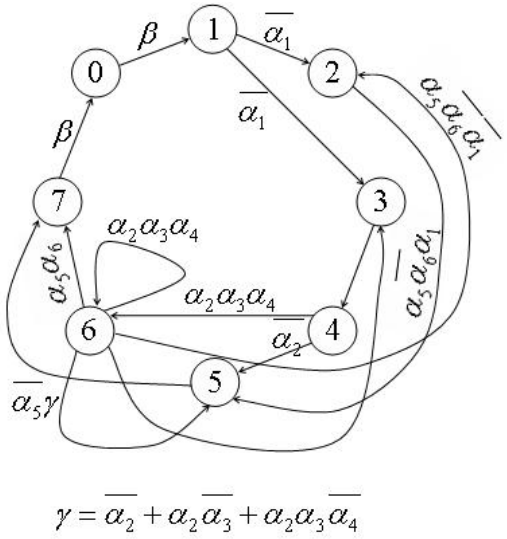


Figure 3. Graph turning Moore automaton

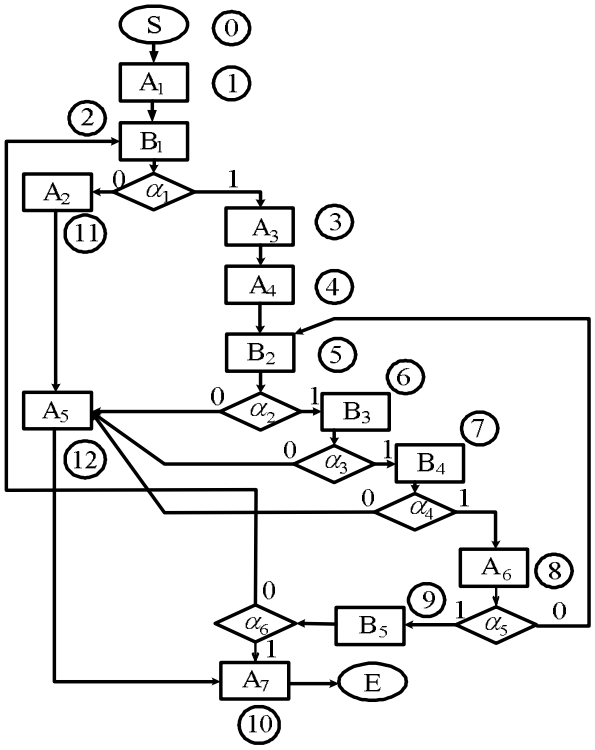


Figure 4. Flow-graph of new control algorithm

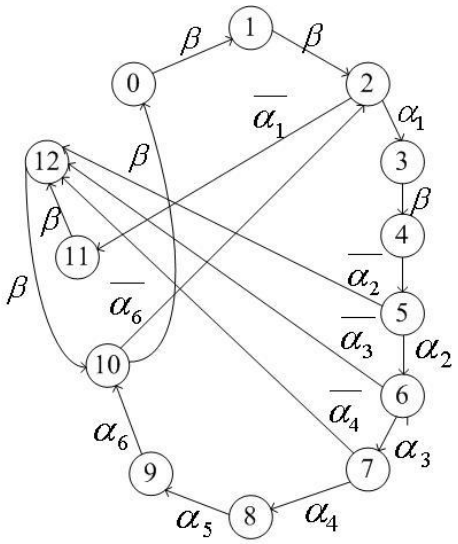


Figure 5. Graph-turning new automaton

To reduce complexity of F1 we may switch to realization by means of programmable logic arrays (PLA) or programmable logic devices (PLD) applying science intensive arrangements to minimize Boolean functions (fig. 5, 6). However for complicated

automatons if m=5 and q=10 the effect from minimization is under 20% and approximates to only a few percents. The second way to structural optimization of PROM is application of decomposition method i.e. partitioning of complicated automatons into a set of simple MPAs (fig. 4).

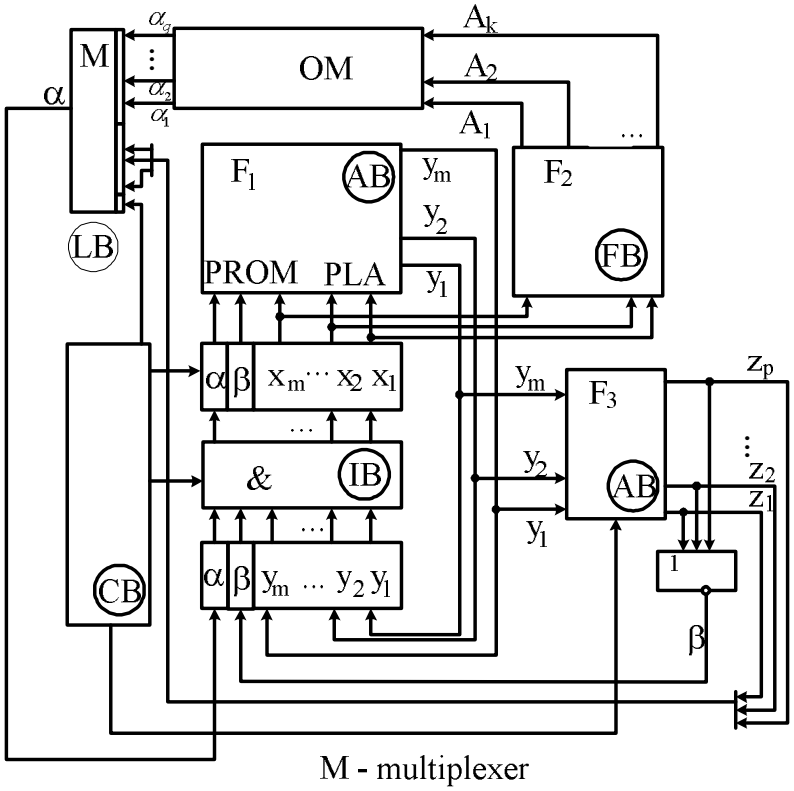


Figure 6. Structural scheme of new automaton

We introduce a new method of complicated MPAs synthesis (fig. 1, 2) which is based on transformation of the specified algorithm flow-graph (AFG). A void action operator A_{k+1} should be inserted after each logical operator α_i in case when output of this α_i is linked with the following α_j without intermediate operator A_p (p – 1, 2, …, k).

A void operator is also inserted before the αi to which control is transferred from several action operators. The modified AFG (fig. 4) allows us to get the transitions graph (fig. 5) in which there are two types of links of a(t) and a(t+1): unconditional β and conditional on single α_j, number (j) of which is completely specified by a(t) code.

Formal description of the new MPA is made by the following equations:

$$a(t+1) = F_1^H(a(t), \beta, \alpha)\ ;\ A(t) = F_2(a(t));\ j = F_3(a(t));\ \text{where “j” is number of “}\alpha\text{”} \quad (2)$$

The length (p) of code $z_1, z_2, \ldots, z_p$ of representation “j” is defined as $p=\log_2 q$. The structural scheme of the MPA (fig. 3) corresponding to equations (2) is presented in fig. 6. As appears from (2), the new system of Boolean functions (F_1^H) of MPA address part does not depend on number (q) of logical conditions, so $V(F_1^H)=m2^{m+2}$. In case (m=5, q=10) we have $L= V(F_1)/ V(F_1^H) = 256$; and for (m=6, q=16) we have $L= 2^{14} \approx 16{,}000$.

Modification of AFG does not break the automaton operation algorithms, but the realization is carried out by MPA structure with much less memory capacity of address part in some hundreds or even thousands times. It is significant that the new structure of MPA will be as efficient in case of realization by PLA or PLD since the number of input variables for F_1^H always equals (m+2); and for practical even the most complicated AFG: $m+2 \leq 8$. As for systems that are not purposed for real-time information processing, instead of hardware realization of MPA by PROM, PLA and PLD we can switch to software realization by microcontroller. For classical structure with $(m+q) \geq 12$ this is problematic, but for the new structure of MPA applying $(m+q) \leq 8$, realization by eight-bit microcontroller is performed by direct reading method.

Thus the new method of MPA synthesis is a breakthrough in the problem of creation of reliable high-speed control facilities for complicated technical systems.

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